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Short-Circuit Failure Mechanisms and Reliability Challenges of Silicon Carbide Power MOSFETs: A Comprehensive Review of Electrical, Thermal, Mechanical Degradation and Failure Analysis Techniques

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Abstract

Silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) have emerged as promising power semiconductor devices for high-power and high-frequency applications owing to their wide bandgap, high critical electric field, superior thermal properties, and low conduction and switching losses. Despite these advantages, short-circuit (SC) reliability remains a critical challenge because these devices experience simultaneous high drain voltage, excessive current density, and rapid temperature rise during fault conditions. Their limited SC withstand capability necessitates a comprehensive understanding of the physical mechanisms responsible for device degradation and catastrophic failure. This review provides a systematic analysis of the coupled electrical, thermal, and mechanical phenomena governing SC failure in SiC MOSFETs, including thermal runaway, gate oxide degradation and breakdown, interlayer dielectric cracking, metallization damage, and threshold-voltage instability. Particular attention is given to the influence of operating conditions, device architecture, and accumulated stress on failure behavior, with comparisons between planar and trench structures and between single-pulse failure and repetitive SC degradation. Furthermore, advanced failure characterization techniques, including electrical parameter measurements, infrared thermography, photo-emission microscopy, lock-in thermography/lock-in thermal emission microscopy (LIT/LITEM), scanning electron microscopy (SEM), and focused ion beam (FIB) analysis, are reviewed for their roles in identifying hotspots, localizing damaged cells, and revealing internal structural defects. Electro-thermal models, technology computer-aided design (TCAD) simulations, and coupled electro–thermal–mechanical approaches are also examined to assess their capabilities and limitations in predicting SC behavior and identifying critical failure locations. Finally, major research challenges and potential strategies for enhancing SC robustness are discussed, including optimized device structures, improved gate oxide reliability, effective thermal management, faster adaptive protection circuits, and reliability-oriented multiphysics modeling. This review establishes an integrated perspective on SC-induced degradation and failure, providing guidance for the development of SiC MOSFETs with improved fault tolerance, enhanced reliability, and greater suitability for demanding power electronic applications.

Keywords: Silicon Carbide MOSFET, Short-Circuit Reliability, Failure Mechanism, Gate Oxide Degradation, Thermal Runaway, Thermo-Mechanical Stress, LITEM, FIB, TCAD Simulation, Reliability Design

1. Introduction

The rapid development of power electronic systems has increased demand for semiconductor devices capable of operating at higher voltages, frequencies, temperatures, and power densities. Conventional silicon (Si) power devices, including Si MOSFETs and insulated-gate bipolar transistors (IGBTs), are approaching fundamental material limitations, particularly under high-voltage and high-temperature conditions. Consequently, wide-bandgap (WBG) semiconductors such as silicon carbide (SiC) have emerged as promising alternatives owing to their superior material properties [1-3].

Compared with Si, SiC exhibits a wider bandgap (~3.2 eV), higher critical electric field, higher thermal conductivity, and

greater high-temperature capability. Its high critical electric field enables thinner drift regions while maintaining high breakdown voltage, thereby reducing specific on-resistance and device dimensions. These characteristics make SiC MOSFETs particularly attractive for high-efficiency, high-power-density, and high-frequency power conversion applications. SiC MOSFETs are increasingly employed in electric vehicle traction inverters, renewable energy converters, railway traction, aerospace power supplies, and industrial motor drives. Their high switching frequency and low switching losses can improve converter efficiency while reducing cooling requirements and system size. Compared with Si IGBTs, which exhibit turn-off tail current due to bipolar conduction, SiC MOSFETs are majority-carrier devices and therefore provide faster switching and lower switching losses, particularly in high-frequency applications.

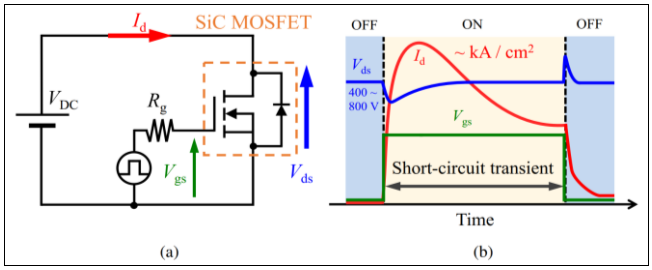


Fig 1: Schematic of (a) a SiC MOSFET short-circuit test circuit and (b) typical short-circuit transient waveforms illustrating the evolution of drain current, drain–source voltage, and gate–source voltage during turn-on, short-circuit, and turn-off operation [5]

Despite these advantages, SiC MOSFETs introduce significant reliability challenges. Their smaller die area, high current density, and high-power density produce severe electrical and thermal stresses during abnormal operating conditions. Short-circuit (SC) reliability as shown in Fig 1, is particularly critical because the device simultaneously experiences high drain voltage and excessive current, resulting in substantial power dissipation within several microseconds. Consequently, SiC MOSFETs generally exhibit shorter short-circuit withstand times than Si IGBTs, making rapid fault detection and protection essential. Therefore, although SiC MOSFETs offer substantial improvements in efficiency, switching performance, and power density, adequate short-circuit robustness remains essential for their reliable deployment. Understanding SC failure mechanisms is necessary for optimizing device structures, improving protection strategies, and developing reliable next-generation SiC power electronic systems [7-9].

2. Short-Circuit Operation in SiC MOSFETs

2.1 Electrical and Thermal Stress During Short Circuit

A short-circuit (SC) event represents one of the most severe operating stresses for SiC MOSFETs because high drain voltage and excessive current occur simultaneously, resulting in extremely high instantaneous power dissipation. During an SC fault, the DC-link voltage remains across the drain-source terminals while the near-zero load impedance allows the drain current to rapidly increase toward the device saturation level [9]. This simultaneous high-voltage and high-current condition produces severe electro-thermal stress and can drive the device toward catastrophic failure.

The instantaneous SC power and accumulated energy can be expressed as:

$$P_{sc}(t) = V_{DS}(t)I_{DS}(t)$$

$$E_{sc} = \int_0^{t_{sc}} V_{DS}(t)I_{DS}(t)dt$$

Where V_{DS}, I_{DS}, and t_{SC} denote the drain-source voltage, drain current, and SC duration, respectively. Since the generated energy is concentrated within a small active volume over a microsecond-scale interval, the junction temperature increases rapidly, producing substantial thermal stress.

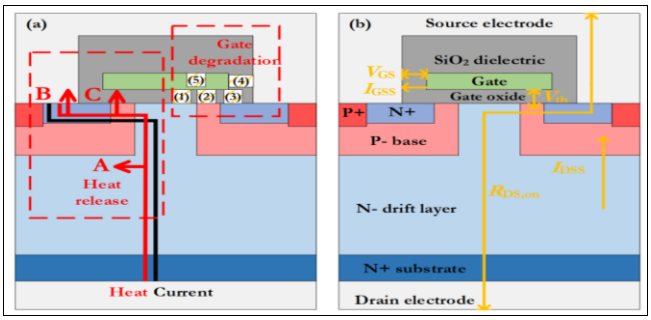


Fig 2: Schematic illustration of (a) heat generation, heat flow, and localized gate degradation during short-circuit operation and (b) the cross-sectional structure of a SiC MOSFET, highlighting key electrical parameters and conduction paths [3]

Compared with Si IGBTs, SiC MOSFETs generally exhibit higher SC current density and lower thermal capacitance because of their smaller chip area. Consequently, the dissipated energy is concentrated within a smaller region, promoting localized hotspots and non-uniform temperature distribution. The SC current is primarily governed by channel saturation and depends strongly on gate-source voltage, threshold voltage, channel mobility, and junction temperature. In particular, increasing the gate voltage raises the saturation current and consequently increases the SC energy dissipation. The high drain voltage also produces strong electric fields in critical device regions, including the gate oxide, JFET region, and drift layer. Combined electrical and thermal stresses can promote carrier injection, interface trap generation, and gate oxide degradation. Moreover, process variations and thermal non-uniformity can produce localized current crowding, resulting in hotspots that initiate gate oxide breakdown, metallization damage, or mechanical cracking. Failure analyses using infrared imaging, LITEM, and FIB have shown that SC damage can be highly localized within individual active regions rather than uniformly distributed across the die. Therefore, SiC MOSFET SC behavior is governed by the coupled effects of high electric field, current density, energy dissipation, and temperature rise. Understanding these interactions is fundamental to identifying SC failure mechanisms and developing more robust device structures and protection strategies. As illustrated in Fig 2(a), short-circuit current generates localized heat within the active region, while the resulting thermal stress can contribute to gate degradation. Fig 2(b) shows the cross-sectional structure of a SiC MOSFET, highlighting the semiconductor layers, gate oxide, and current conduction paths that influence electrical and thermal stress distribution during SC operation [10].

During a short-circuit (SC) event, a SiC MOSFET experiences extremely high power density because high

drain-source voltage and current occur simultaneously. The dissipated electrical energy is rapidly converted into heat within the active region, producing a sharp increase in junction temperature. The SC energy can be expressed as:

$$E_{sc} = \int_0^{t_{sc}} V_{DS}(t) I_{DS}(t) dt$$

Where V_{DS}, I_D, and t_{sc} represent the drain-source voltage, drain current, and SC duration, respectively.

Because SC events typically last only several microseconds, heat transfer from the die to the package and heat sink is limited. The device therefore experiences approximately adiabatic heating, and the temperature rise can be estimated as:

$$\Delta T = \frac{E_{sc}}{C_{th}}$$

Where C_{th} is the effective thermal capacitance. The small die area and high current density of SiC MOSFETs concentrate the dissipated energy within a limited volume, resulting in a rapid temperature rise compared with Si IGBTs [11].

Under destructive SC conditions, the junction temperature may reach levels sufficient to cause secondary physical damage. Experimental investigations have reported aluminum source metallization melting, deformation, and internal structural degradation, confirming the extreme temperatures generated during SC failure. Furthermore, thermal stress is generally non-uniform across the die. Current crowding, cell variations, and non-uniform thermal resistance can produce localized hotspots that accelerate gate oxide degradation, dielectric damage, and metallization failure. Failure analysis using infrared thermography, LITEM, and FIB has confirmed that SC damage is frequently concentrated in localized active regions. Therefore, transient thermal stress is a major factor governing the SC withstand capability of SiC MOSFETs. Achieving low conduction resistance while maintaining sufficient thermal robustness remains an important challenge in SiC MOSFET design [12].

2.2 Current Saturation and Temperature Feedback During Short Circuit

During a short-circuit (SC) event, the drain current of a SiC MOSFET is mainly limited by channel saturation and is strongly influenced by gate-source voltage, threshold voltage, carrier mobility, and junction temperature. Consequently, SC current evolution is closely coupled with the thermal response of the device. As junction temperature increases, carrier mobility decreases due to enhanced phonon scattering, tending to reduce the drain current. Conversely, the threshold voltage decreases with temperature, increasing channel inversion charge. The competition between these effects determines the temperature dependence of the saturation current. In many SiC MOSFETs, mobility degradation dominates, resulting in a negative temperature coefficient and a gradual reduction in drain current after the initial SC peak [14].

However, under severe stress, increasing temperature can enhance leakage current and carrier generation, producing additional power dissipation. This positive electro-thermal feedback further increases junction temperature and may eventually lead to thermal runaway and catastrophic failure. In high-voltage SiC MOSFETs, impact ionization can also generate excess carriers and potentially activate the intrinsic parasitic bipolar transistor. Such parasitic conduction, combined with positive thermal feedback, can accelerate SC failure.

Therefore, SC withstand capability is governed by the interaction between current saturation, temperature-dependent device characteristics, and electro-thermal feedback. Understanding these coupled mechanisms is essential for improving device robustness and short-circuit protection [13].

3.1 Thermal Runaway Failure Mechanism

Thermal runaway is a major catastrophic failure mechanism in SiC MOSFETs during short-circuit (SC) operation. Under SC conditions, high drain–source voltage and excessive current occur simultaneously, producing substantial instantaneous power dissipation, expressed as Psc=Vds*Ids, and rapid Joule heating within the active region. Because SC events typically last only a few microseconds, heat transfer to the package and heat sink is limited, resulting in a sharp rise in junction temperature. This temperature increase can intensify leakage current and carrier generation, leading to additional power dissipation and positive electrothermal feedback. As illustrated in Fig 3, the drain-current and gate-voltage waveforms demonstrate the transient behavior preceding thermal runaway under different gate-drive conditions at DC=800V. The abrupt changes in the measured waveforms near the end of the SC pulse indicate the onset of thermal instability and device failure. These results highlight the influence of gate-drive conditions on SC behavior and the importance of limiting the duration and energy of fault events.

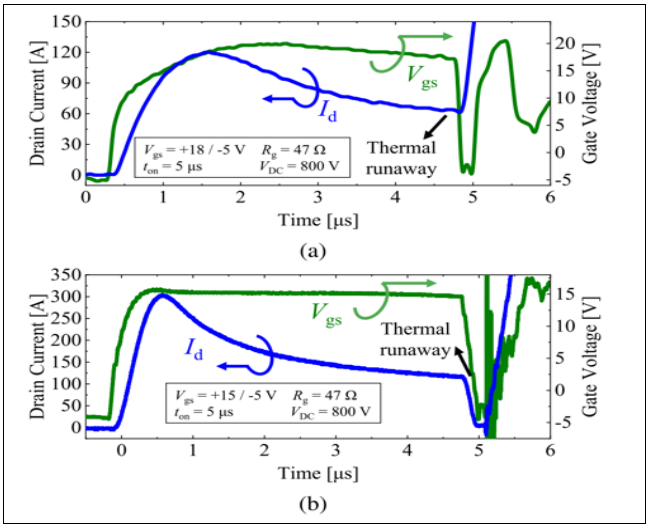


Fig 3: Short-circuit current, drain–source voltage, and gate–source voltage waveforms illustrating thermal runaway in SiC MOSFETs under different gate-drive conditions: (a) Vgs=+18/-5 V and (b) Vgs=+15/-5 V, at Vdc=800 V [34]

Once electrothermal feedback becomes dominant, thermal instability can lead to irreversible device failure. Experimental investigations have associated thermal runaway with drain–source short circuits, semiconductor damage, and metallization degradation. Under destructive conditions, melting of the aluminum source metallization

has also been observed, indicating extremely high local temperatures. The onset of thermal runaway depends strongly on operating conditions and device design, particularly DC-link voltage, gate bias, initial junction temperature, and device structure. Higher electrical stress generally increases SC energy dissipation and reduces the short-circuit withstand capability [34].

3.2 Gate Oxide Degradation and Breakdown

Gate oxide reliability is a critical limitation of SiC MOSFETs under short-circuit (SC) operation because the SiC/SiO_2 interface contains a relatively high density of defects and interface traps. During SC stress, the gate dielectric is simultaneously exposed to high electric field and elevated temperature, accelerating defect generation and oxide degradation. The oxide electric field can be approximated as Eox=vg/tox, where Vg and tox are the gate voltage and oxide thickness, respectively. Under severe SC conditions, the combined electrical and thermal stresses further increase the susceptibility of the gate dielectric to degradation.

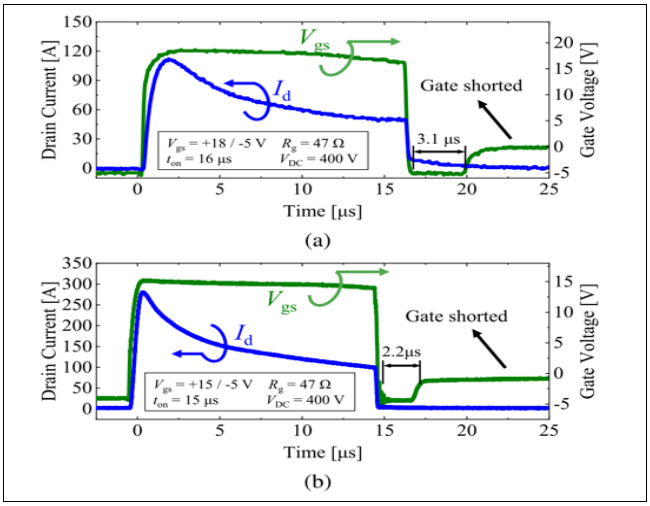


Fig 4: Short-circuit current, drain–source voltage, and gate–source voltage waveforms illustrating thermal runaway in SiC MOSFETs under different gate-drive conditions: (a) Vgs=+18/-5 V and (b) Vgs=+15/-5 V, at Vdc=400 V [34]

Fig 4 illustrates the short-circuit current and gate-voltage transients under different gate-drive conditions at a DC-link voltage of 400 V. The abrupt waveform changes associated with the marked gate-short events demonstrate the severity of the electrical stress and the potential for irreversible device failure during SC operation [34]. Several mechanisms contribute to this degradation. High electric fields can accelerate carriers near the channel and drain regions, resulting in hot-carrier injection into the oxide and subsequent generation of oxide and interface traps. Charge trapping and detrapping at the SiC/SiO_2 interface can modify the threshold voltage and device characteristics. At sufficiently high oxide fields, Fowler–Nordheim tunneling may contribute to carrier transport through the dielectric, while pre-existing and stress-induced defects can facilitate trap-assisted tunneling and the formation of conductive leakage paths.

Progressive gate oxide degradation is generally reflected by an increase in gate leakage current Igss, threshold-voltage Vth instability, reduced effective gate voltage, and deterioration of gate controllability. Experimental studies have identified increasing Igss as an important indicator of SC-induced gate dielectric degradation. Under severe stress, accumulated oxide damage may eventually form permanent conductive paths, resulting in gate-source breakdown and irreversible device failure [15].

3.3 Interlayer Dielectric Cracking and Mechanical Failure

Recent investigations have shown that short-circuit (SC) failure in SiC MOSFETs can originate from thermo-mechanical degradation rather than conventional electrical breakdown of the gate oxide. During an SC event, the extremely high power density produces a rapid temperature rise within the die. Differences in the coefficients of thermal expansion among SiC, dielectric layers, and metal electrodes generate substantial mechanical stress. When this stress exceeds the mechanical strength of the interlayer dielectric, cracks can develop and propagate within the damaged region. As shown in Fig 5, the cross-sectional SEM images reveal cracks in the interlayer dielectric near the polysilicon gate and source metallization. These observations provide physical evidence of structural damage in the gate region and illustrate how short-circuit-induced thermo-mechanical stress can compromise dielectric integrity [34].

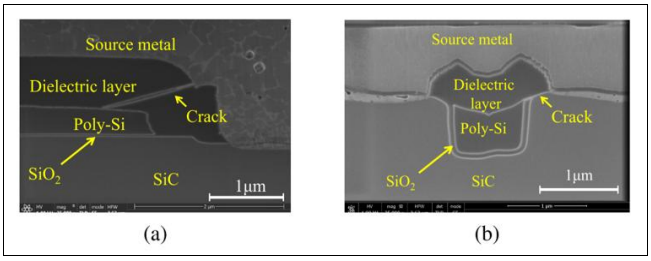


Fig 5: Cross-sectional SEM images showing short-circuit-induced cracking of the interlayer dielectric in SiC MOSFETs: (a) crack formation near the polysilicon gate and source metallization; (b) corresponding dielectric cracking and structural damage in the gate region [34]

These cracks can provide pathways for molten or displaced source metallization to penetrate toward the gate structure, progressively reducing electrical isolation between the gate and source and ultimately producing a gate-source short circuit. This mechanism is therefore characterized by a sequence of rapid heating, thermal expansion mismatch, dielectric cracking, metal penetration, and loss of gate-source isolation. Unlike conventional gate oxide breakdown, the primary damage originates from thermo-mechanical fracture. Its occurrence is strongly influenced by local temperature, hotspot formation, and SC duration, demonstrating the important role of mechanical stress in SiC MOSFET short-circuit reliability [16].

3.4 Metallization Failure

Metallization degradation is an important failure mechanism during severe short-circuit (SC) events because the aluminum source electrode and associated interconnects are exposed to extreme thermal stress near the active region. When the local temperature approaches or exceeds the aluminum melting point, the source metallization can melt and redistribute, causing permanent structural damage. As shown in Fig 6, the SEM and FIB cross-sectional images reveal several forms of short-circuit-induced physical damage, including gate oxide failure, cracks in the gate

region, and localized internal structural degradation. These observations demonstrate the severe thermal and structural stresses associated with SC events and provide microstructural evidence of damage near the gate and metallization regions [25].

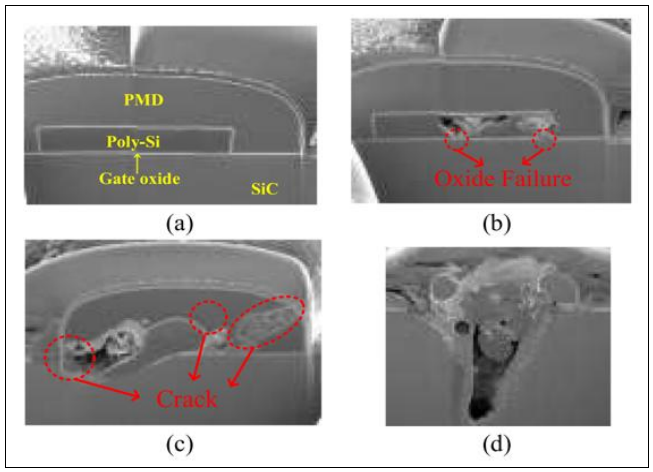


Fig 6: SEM and FIB cross-sectional images illustrating short-circuit-induced metallization and structural degradation in SiC MOSFETs: (a) cross-sectional device structure showing the PMD, polysilicon gate, gate oxide, and SiC substrate; (b) gate oxide failure; (c) crack formation in the gate region; and (d) localized internal structural damage following short-circuit stress [25]

Rapid thermal expansion and melting may also reconstruct the source electrode morphology, producing irregular surfaces and electrical discontinuities. In addition, high temperatures can promote metal migration and the formation of unwanted conductive paths, while repeated thermal stress may generate voids that increase contact resistance and accelerate degradation. Microstructural investigations using SEM and FIB have revealed aluminum deformation, metal particles, and structural abnormalities after SC failure, confirming the significant contribution of metallization degradation to catastrophic device failure.

3.5 Threshold Voltage Instability

Threshold voltage Vth instability is an important indicator of progressive SiC MOSFET degradation under repetitive short-circuit (SC) stress and is primarily associated with charge trapping and detrapping in the gate oxide and SiC/SiO_2 interface. A negative Vth shift is generally attributed to hole trapping caused by high-energy carrier generation and injection into the oxide, which can reduce the turn-on voltage and degrade gate stability.

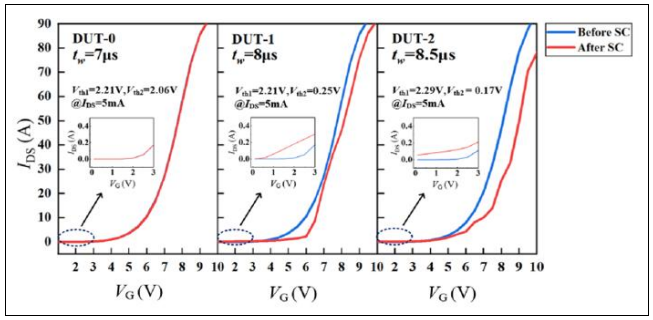


Fig 7: Transfer characteristics of three SiC MOSFET devices under test (DUTs) before and after short-circuit stress, illustrating threshold-voltage shifts associated with SC-induced degradation [19]

As shown in Fig 7, the transfer characteristics of the three devices exhibit changes after SC stress compared with their initial characteristics. These shifts in the (I_D)–(V_G) curves indicate variations in threshold-voltage behavior and demonstrate the influence of SC stress on the electrical characteristics of SiC MOSFETs [19]. Conversely, a positive Vth shift is associated with electron trapping at oxide defects or interface states, potentially increasing the turn-on voltage and conduction losses. The direction and magnitude of the Vth shift depend strongly on junction temperature, SC pulse duration, gate-source voltage, number of stress cycles, and gate oxide quality. Repetitive SC studies have therefore identified Vth, together with gate and drain leakage currents, as useful electrical indicators for monitoring progressive SiC MOSFET degradation.

4. Influence of Device Structure on Short-Circuit Reliability

The short-circuit (SC) reliability of SiC MOSFETs is strongly influenced by device structure, including cell design, gate configuration, current distribution, and thermal behavior. Technological development has primarily targeted lower specific on-resistance Rds (on), higher current capability, and improved switching performance. However, these improvements can increase current density, electric-field concentration, and thermal stress during SC operation, creating a trade-off between electrical performance and fault robustness.

Commercial SiC MOSFETs mainly employ planar- and trench-gate structures. Planar devices benefit from mature fabrication technology and generally established SC robustness, whereas trench MOSFETs achieve lower channel resistance and higher channel density. However, trench architectures can introduce localized electric-field concentration and increased gate oxide stress, particularly near trench corners. Consequently, optimizing device structure to achieve low conduction losses while maintaining adequate SC robustness remains a key challenge in SiC MOSFET development [21].

4.1 Planar SiC MOSFETs

Planar SiC MOSFETs represent an established commercial device architecture and have been extensively investigated for short-circuit (SC) reliability. In this structure, the gate is located on the device surface, with current flowing through the lateral inversion channel before entering the vertical drift region. Compared with trench architectures, planar devices generally exhibit lower electric-field concentration because of the absence of sharp trench corners, reducing localized gate oxide stress during high-voltage operation. However, their relatively low SiC/SiO_2 interface mobility results in higher channel resistance. Increasing cell density and reducing channel length can lower conduction losses but may increase SC current density, power dissipation, and junction temperature, thereby reducing SC withstand capability.

Under SC conditions, planar SiC MOSFETs can fail through thermal runaway, gate oxide or dielectric degradation, and metallization damage. Experimental studies have reported both gate–source failure associated with dielectric damage and drain–source failure resulting from severe thermal destruction, with the dominant mechanism depending on DC-link voltage, gate bias, SC duration, and device design. Although planar MOSFETs generally exhibit higher on-state

resistance than trench devices, their simpler gate geometry and comparatively moderate electric-field concentration can provide competitive SC robustness. The cross-sectional SEM images in Fig 8 illustrate localized dielectric cracking, metallization damage, and structural degradation following SC stress in a trench SiC MOSFET. These observations demonstrate the importance of gate-region integrity and thermo-mechanical stress in determining SC reliability, providing a useful comparison for understanding failure mechanisms across different SiC MOSFET architectures [28].

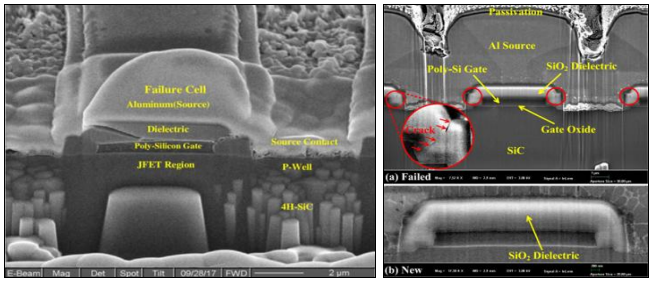


Fig 8: Cross-sectional SEM image showing short-circuit-induced cracking of the interlayer dielectric near the polysilicon gate and source metallization in a trench SiC MOSFET [28]

4.2 Trench SiC MOSFETs

Trench SiC MOSFETs were developed to reduce the conduction limitations of planar structures by increasing channel density and lowering channel resistance. In this architecture, the gate is vertically embedded in the semiconductor and the channel forms along the trench sidewalls, enabling lower specific on-resistance and higher current capability at a given breakdown voltage. However, trench architectures introduce additional short-circuit (SC) reliability concerns. Electric-field concentration near trench corners and the trench bottom can increase gate oxide stress, particularly under simultaneous high-field and high-temperature SC conditions. Consequently, oxide degradation, interface trap generation, threshold-voltage instability, and localized thermal damage may occur. Careful optimization of trench geometry, oxide design, and electric-field shielding is therefore essential for maintaining gate reliability [26-27]. The structural damage and elemental distribution observed after SC stress provide further evidence of these reliability concerns. As shown in Fig 9(a), energy-dispersive X-ray (EDX) mapping reveals the distribution of aluminum around the damaged dielectric region. The elemental composition profile in Fig 9(b) identifies a localized aluminum peak near the crack, indicating metal accumulation in the damaged region. These observations support the role of metallization redistribution and dielectric damage in trench-device failure and illustrate how localized structural defects can compromise gate-region integrity [34].

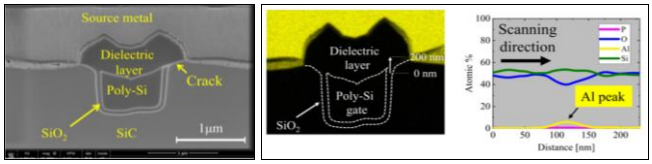


Fig 9: Energy-dispersive X-ray (EDX) analysis of a trench SiC MOSFET after short-circuit stress: (a) aluminum elemental mapping showing metal distribution around the damaged dielectric region; (b) elemental composition across the crack, highlighting the localized aluminum peak [34]

Recent studies of commercial SiC MOSFETs indicate that trench devices can achieve competitive or improved SC robustness when appropriately optimized. Advanced trench geometries, improved thermal distribution, and optimized cell designs can suppress hotspot formation and enhance SC capability. Thus, the SC reliability of trench MOSFETs is strongly dependent on device architecture and fabrication technology rather than the trench structure alone.

4.3 Comparison Between Planar and Trench Structures

The short-circuit (SC) reliability of planar and trench SiC MOSFETs reflects a fundamental trade-off between conduction performance and fault robustness. Planar devices feature a simpler gate structure and lower electric-field concentration, providing relatively established gate oxide reliability, but generally exhibit higher channel resistance and require a larger chip area. In contrast, trench MOSFETs achieve lower specific on-resistance Rds (on), higher channel density, and reduced die area, resulting in improved conduction performance. However, electric-field concentration at trench corners increases gate oxide stress and sensitivity to oxide defects. Therefore, neither architecture provides universally superior SC reliability; the resulting robustness depends strongly on device geometry, oxide design, current distribution, and thermal management [33-35]. Table 1 summarizes the structural, electrical, and reliability differences between the two architectures. However, structural characteristics alone cannot determine SC robustness, which also depends on operating conditions and device design.

Table 1: Comparison of structural characteristics, conduction performance, and short-circuit reliability of planar and trench SiC MOSFETs

Parameter	Planar SiC MOSFET	Trench SiC MOSFET
Channel structure	Surface inversion channel	Vertical trench channel
On-resistance	Higher	Lower
Cell density	Lower	Higher
Electric field concentration	Lower	Higher at trench corners
Gate oxide stress	Moderate	Higher
Short-circuit robustness	Generally better established	Highly dependent on design
Main reliability concern	Thermal stress and oxide degradation	Trench oxide stress and localized failure

Recent cross-vendor investigations have shown that the short-circuit capability is not determined only by planar or trench classification but also by generation, die size, thermal design, and manufacturing process. Some advanced trench devices demonstrate comparable or even improved short-circuit performance compared with planar devices due to better current distribution and thermal management. Therefore, future SiC MOSFET development requires a balanced optimization between conduction performance and short-circuit reliability. Structural improvements such as optimized trench geometry, improved gate oxide processes, shielding regions, and advanced cell designs are essential to achieve both low losses and high fault tolerance. Table 2 summarizes reported SC withstand times (SCWTs) and associated failure mechanisms under different test conditions. The results indicate that increasing DC-link voltage can reduce SCWT and trigger different failure mechanisms, including thermal runaway, gate-oxide

breakdown, dielectric fracture, and parasitic BJT activation [22-24, 32].

Table 2: Short-circuit withstand capability and failure mechanisms of SiC MOSFETs under different test conditions

Ref.	Device structure	Short-circuit withstand time (SCWT)	Main failure mechanism
[21]	1200 V planar	Depends on test conditions	Gate dielectric breakdown and thermal runaway; case temperature significantly affects robustness.
[30]	1200 V planar; 650 V symmetrical trench	Planar: 19.5/9.5 µs; trench: 20.4/8.6/7.5 µs	High DC-link voltage promotes thermal runaway; failure depends on voltage and device structure.
[22]	1200 V symmetrical trench	20.4 µs at 400 V; 5.7 µs at 800 V	Conductive path between gate and source at 400 V; thermal runaway and possible parasitic BJT activation at 800 V.
[23]	1200 V planar and asymmetrical trench	Planar: 16/5 µs; trench: 15/5 µs	Dielectric fracture associated with high mechanical stress at 400 V; parasitic BJT activation at 800 V.
[24]	1200 V symmetrical trench	Device 1: 15/10 µs; Device 2: 32/4 µs (400/800 V)	SiO_2 rupture at 400 V and thermal runaway at 800 V.
[32]	1200 V symmetrical and asymmetrical trench	Symmetrical: 15/8.5/2.5 µs; asymmetrical: 15/8.5/5.8 µs (400/600/800 V)	Thermal runaway in symmetrical trench devices; gate failure at 400 V and thermal runaway at 800 V in asymmetrical devices.
[35]	1200 V planar and symmetrical trench devices	Depends on device and test conditions	Gate failure, thermal runaway, and drain–source short circuit; behavior depends on chip size, doping, and topology.
[41, 42]	650 V planar and symmetrical trench	Depends on test conditions	Planar devices showed greater robustness than trench devices in the reported comparison.
[14]	Planar and symmetrical trench	Planar: 14 µs at 900 V; trench: 19 µs at 650 V	Thermal runaway in planar devices; gate oxide breakdown in trench devices.

5. Single Short-Circuit Failure vs. Repetitive Short-Circuit Degradation

Short-circuit (SC) reliability of SiC MOSFETs can be evaluated through two aspects: single SC event failure and repetitive SC degradation. A single SC event determines the ultimate withstand capability of the device, while repetitive SC stress reveals progressive degradation caused by accumulated electrical, thermal, and mechanical stresses [37].

5.1 Single Short-Circuit Event Failure

During a single short-circuit (SC) event, simultaneous high drain voltage and excessive current produce substantial power dissipation Psc=Vds*Id, causing a rapid junction temperature rise within the microsecond-scale fault duration. If the dissipated energy exceeds the device limit, irreversible failure occurs. High power density can trigger thermal runaway, semiconductor destruction, and source metallization melting. In addition, rapid heating and thermal expansion mismatch can induce dielectric cracking, allowing metal penetration and eventual gate-source short circuit. Simultaneous high electric field and temperature may further accelerate gate oxide degradation and breakdown. Thus, single-event SC failure typically results from coupled thermal, mechanical, and dielectric stresses.

5.2 Repetitive Short-Circuit Aging

Although individual short-circuit pulses may not cause immediate failure, repetitive SC stress progressively degrades SiC MOSFETs through oxide damage, interface defects, and structural deterioration. Charge trapping and detrapping in the gate oxide and SiC/SiO_2 interface can produce positive or negative threshold-voltage shifts depending on the stress conditions.

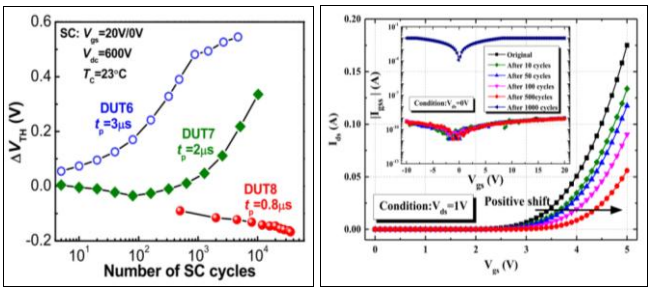


Fig 10: Threshold-voltage shift as a function of repetitive short-circuit (SC) cycles for planar-gate SiC MOSFETs under different SC pulse durations, illustrating the dependence of degradation on accumulated stress

Repetitive stress also increases gate leakage current, indicating progressive dielectric degradation, while increased drain leakage current reflects deterioration of blocking capability. Furthermore, interface and contact degradation can increase, resulting in higher conduction losses and additional thermal stress. Therefore, Vth, Igss, Igss and Idss are important indicators for evaluating repetitive SC-induced degradation.

6. Short-Circuit Failure Analysis Techniques

Electrical characterization is a primary method for assessing SiC MOSFET degradation before and after SC stress. Transfer characteristics reveal changes in threshold voltage, transconductance, and channel behavior, while gate leakage current indicates gate-oxide degradation and leakage-path formation. Drain leakage current reflects deterioration of blocking capability, whereas changes in on-state resistance can indicate channel, interface, or contact degradation. Threshold voltage is particularly sensitive to charge trapping at the SiC/SiO_2 interface [38].

6.1 Electrical Characterization

The effects of repetitive SC stress can also be evaluated through switching waveforms. As shown in Fig 11, the turn-on and turn-off characteristics change with increasing SC stress cycles, including variations in gate voltage, drain–source voltage, and drain current. These changes indicate progressive alterations in the device's dynamic switching behavior and demonstrate the importance of waveform analysis in evaluating SC-induced degradation [17]. Monitoring these electrical parameters during repetitive SC testing enables potential reliability issues to be identified before catastrophic failure.

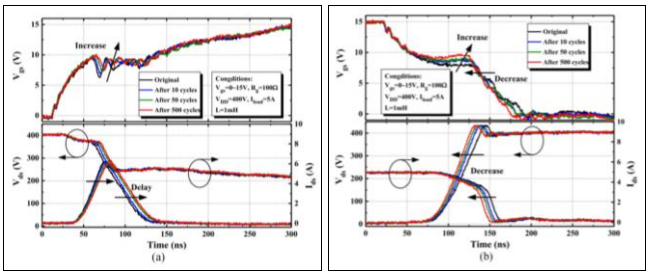


Fig 11: Turn-on (a) and turn-off (b) switching waveforms of a planar-gate SiC MOSFET after different numbers of repetitive short-circuit stress cycles, illustrating changes in gate voltage, drain–source voltage, and drain current associated with progressive device degradation [17]

6.2 Infrared Thermography

Infrared (IR) thermography is widely used to characterize the thermal behavior of SiC MOSFETs during short-circuit (SC) stress. IR imaging visualizes surface temperature distribution and identifies localized hotspots associated with excessive power dissipation. By correlating thermal concentrations with the final failure location, this technique helps distinguish localized thermal damage from more uniform die heating and provides insight into the thermal origins of SC-induced failure [40].

As illustrated in Fig 12, lock-in thermal emission microscopy (LITEM) reveals localized hotspots in commercial SiC MOSFETs following short-circuit stress. The images show that thermally active regions can be concentrated in specific areas of the device rather than distributed uniformly across the die. This spatial information helps identify potential failure sites and supports the subsequent investigation of damaged regions using structural analysis techniques [35].

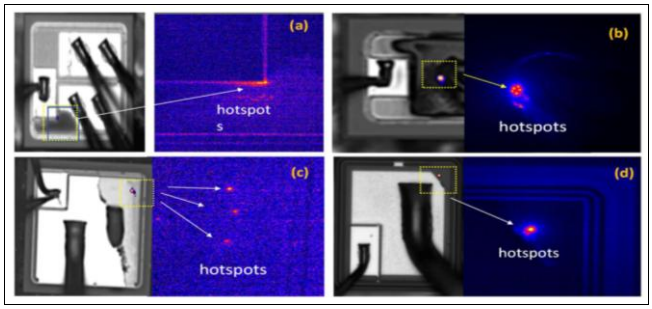


Fig 12: Lock-in thermal emission microscopy (LITEM) images showing localized short-circuit-induced hotspots in commercial SiC MOSFETs: (a) Cree-9C, (b) Cree-3G, (c) Infineon Trench-1G, and (d) Rohm Trench-3G devices, illustrating the localization of damaged active regions following metal removal [35]

6.3 Photo Emission Microscopy (PEM)

Photo emission microscopy (PEM) is an optical failure analysis technique that detects localized photon emission associated with abnormal electrical activity in semiconductor devices. It is particularly useful for identifying leakage-current sites, damaged active regions, and potential failure locations. Compared with conventional optical inspection, PEM provides greater sensitivity to microscopic electrical defects. Mbarek *et al*. demonstrated its effectiveness, combined with electrical characterization, for localizing damaged cells in SiC MOSFETs after short-circuit stress.

6.4 Lock-in Thermography / Lock-in Thermal Emission Microscopy (LITEM)

Lock-in thermography and lock-in thermal emission microscopy (LITEM) are sensitive thermal imaging techniques for localizing heat sources associated with electrical defects. LITEM provides high-resolution thermal mapping of hotspots and damaged cells, which is particularly valuable because short-circuit (SC) damage may remain confined to localized regions of the SiC MOSFET die. Makhdoom *et al*. combined LITEM with optical inspection and FIB analysis to localize damaged active and gate-related regions in commercial 1.2-kV SiC MOSFETs, demonstrating its effectiveness in correlating electrical degradation with physical failure locations.

6.5 SEM and FIB Cross-sectional Analysis

Scanning electron microscopy (SEM) and focused ion beam (FIB) analysis reveal structural damage following short-circuit (SC) failure, including dielectric cracking, gate-oxide damage, metal migration, and metallization deformation. As shown in Fig 13, FIB cross-sectional images reveal localized dielectric cracking near the active cells of planar and trench SiC MOSFETs. These observations highlight the importance of dielectric integrity in SC reliability. Combined with electrical characterization and PEM/LITEM imaging, SEM/FIB analysis provides an effective approach for identifying the physical origins of SC failure [35, 41].

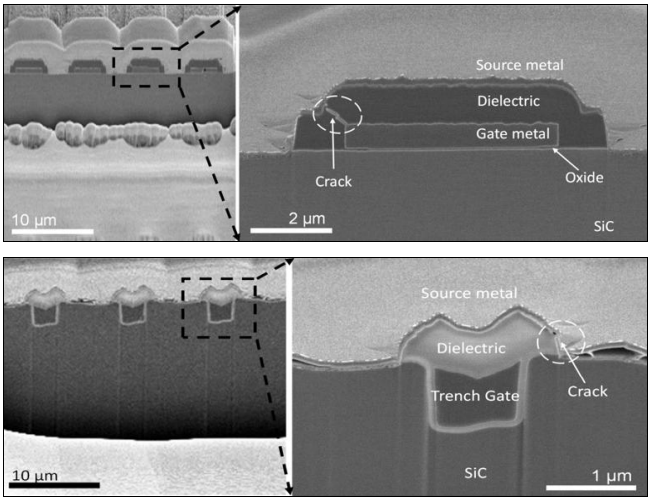


Fig 13: Focused ion beam (FIB) cross-sectional analysis of failed SiC MOSFETs showing abnormal active cells and short-circuit-induced cracking in the dielectric and pre-metal dielectric layers of a Cree-2G device and an Infineon Trench-1G device [35]

7. Modeling Approaches for Short-Circuit Failure Prediction

Accurate prediction of short-circuit (SC) failure in SiC MOSFETs requires modeling approaches capable of describing the interaction between electrical stress, heat generation, and structural degradation. Since SC failure occurs within a few microseconds and involves complex coupled phenomena, numerical models are essential for understanding internal device behavior that cannot be directly measured experimentally. The major modeling approaches include electro-thermal models, TCAD simulations, and multi-physics electro–thermal–mechanical models.

7.1 Electro-Thermal Models

Electro-thermal models are widely used to predict energy dissipation and temperature evolution during short-circuit (SC) operation. The dissipated energy is:

$$E_{sc} = \int_0^{t_{sc}} V_{DS}(t) I_{DS}(t) dt$$

Produces a rapid junction temperature rise that directly influences current saturation, leakage, and failure behavior. By coupling electrical device equations with thermal networks, these models estimate junction temperature, heat distribution, and SC withstand capability under different DC-link voltages, gate biases, initial temperatures, and SC durations. However, conventional electro-thermal models have limited capability to describe microscopic degradation mechanisms such as interface trap generation, oxide damage, and mechanical cracking.

SiC MOSFET short-circuit (SC) failure involves coupled electrical, thermal, and mechanical phenomena, requiring multi-physics modeling for comprehensive failure prediction. High voltage and current generate intense Joule heating, while the resulting temperature rise produces thermo-mechanical stress through material expansion mismatch, potentially causing dielectric cracking, oxide damage, and metallization deformation. As shown in Fig 14, simulated temperature distributions reveal localized heating in both planar and trench SiC MOSFETs at the end of the SC transient. The different temperature patterns highlight the influence of device architecture on heat concentration and thermal stress. Because SC failure involves coupled electrical, thermal, and mechanical phenomena, integrating thermal analysis with TCAD simulations and mechanical-stress modeling can improve failure prediction. Future models should balance physical accuracy and computational efficiency for practical reliability assessment [34, 40].

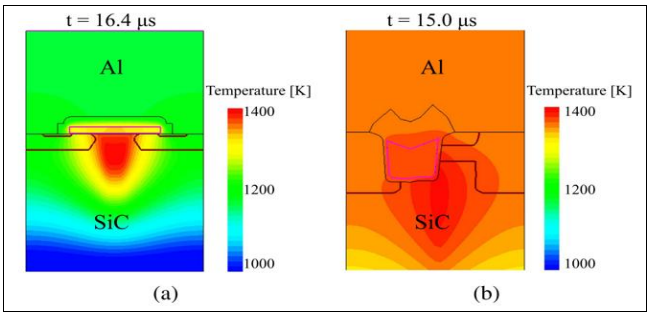


Fig 14: Simulated temperature distributions at the end of a 400-V short-circuit transient in (a) a planar SiC MOSFET at t = 16.4us and (b) a trench SiC MOSFET at t = 15.0us [34]

7.2 TCAD Simulation

Technology Computer-Aided Design (TCAD) simulation provides detailed insight into the internal physical behavior of SiC MOSFETs during short-circuit (SC) operation by coupling electrical, thermal, and carrier transport models. TCAD can evaluate non-uniform current distribution and hotspot formation, electric-field concentration in the gate oxide and drift region, and interface-trap effects associated with threshold-voltage shift, mobility degradation, and leakage current. Coupled thermal simulations further identify regions susceptible to excessive temperature rise and thermal runaway [34]. Demonstrated that current distribution, electro-thermal feedback, interface effects, and structural parameters strongly influence the SC capability of high-voltage SiC MOSFETs. Despite its physical accuracy, the computational complexity of TCAD limits its use in large-scale reliability and system-level simulations.

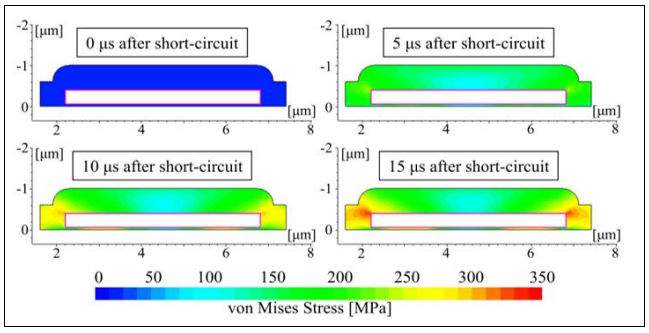


Fig 15: TCAD-simulated von Mises stress distribution in a planar SiC MOSFET during a 400-V short-circuit transient: (a) stress evolution at a selected point and (b) spatial stress distributions at 0, 5, 10, and 15 µs after the short-circuit event [34]

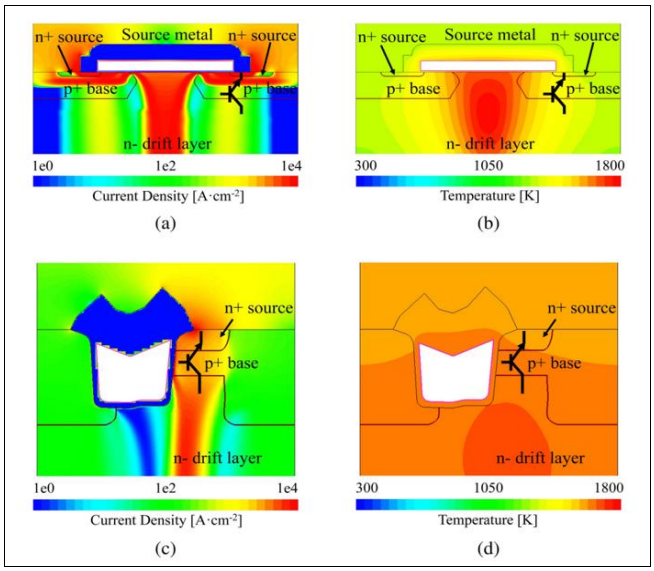


Fig 16: TCAD-simulated (a, c) current density and (b, d) temperature distributions in planar and trench SiC MOSFETs during short-circuit operation, illustrating differences in current crowding, hotspot formation, and thermal distribution between the two device structures [34]

8. Conclusion

Short-circuit (SC) reliability remains a major challenge in the development and application of silicon carbide (SiC) MOSFETs for high-power systems. This review has examined the electrical, thermal, and mechanical processes governing SC-induced degradation and failure. The principal failure mechanisms include thermal runaway, gate-oxide degradation, interlayer dielectric cracking, metallization damage, and threshold-voltage instability. Their occurrence and severity depend on device architecture, operating conditions, manufacturing technology, and thermal management. Advanced characterization techniques, including electrical analysis, infrared thermography, photo-emission microscopy, lock-in thermal emission microscopy (LITEM), scanning electron microscopy (SEM), and focused ion beam (FIB) analysis, provide complementary insights into electrical degradation, hotspot localization, and physical damage. Electro-thermal

models, technology computer-aided design (TCAD) simulations, and multiphysics approaches further improve understanding of the coupled processes responsible for SC failure. Comparisons between planar and trench structures also demonstrate the importance of balancing conduction performance with gate-oxide integrity and short-circuit robustness. Future research should focus on optimizing device structures, improving gate-dielectric reliability, enhancing thermal management, developing accurate failure-prediction models, and implementing fast adaptive protection strategies. Integrating robust device design, comprehensive failure analysis, and reliable protection circuits will be essential for improving SC withstand capability and advancing the long-term reliability of next-generation SiC MOSFETs in demanding power-electronic applications.

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