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Two-Stage Low-Noise Amplifier; Simulation and Comparison Based BJT at 900-1000MHz

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Abstract
The paper presents a simulation study on the design of a two-stage low-noise amplifier (LNA) using a (BJT). The simulation results were compared to key performance metrics at frequencies of 900 MHz and 1000 MHz. At 900 MHz, the amplifier achieves a gain of 25.7 dB, a noise figure of 4.6 dB, and stability of 7.6 dB. At 1000 MHz, the gain decreases to 17.6 dB, the noise figure improves to 1.8 dB, and stability increases to 9.4 dB.

Keywords: LNA, BJ Transistor, Simulation, Microwave Office, Amplifier

1. Introduction

The Low Noise Amplifier (LNA) is designed to amplify small signals with moderate gain while minimizing the noise figure [1]. Achieving low noise and maximum gain simultaneously can be quite challenging. The main criteria for assessing the performance of an LNA include gain, voltage standing wave ratio, and NF [2]. Additionally, an effective LNA should exhibit good impedance matching, stability, and linearity within its operating band [3]. LNAs are commonly used in various applications, including wireless local area networks, Bluetooth, global positioning systems, and satellite communications. Research indicates that using a two-stage cascade method in LNA design can yield an average gain of ~28 dB [4]. This approach not only facilitates higher transistor stability but also improves performance [5]. In the design of an LNA, it is essential to include an impedance adjustment circuit to optimize power transfer from the source to the load. However, the use of LC components at high frequencies can introduce parasitic effects that need to be managed. In a two-stage LNA design, the first stage employs noise-canceling and transconductance boosting techniques to achieve favorable noise figures, wideband input matching, and low power consumption. The second stage consists of a fully differential cascode amplifier that provides additional voltage gain.

Our work focuses on designing a (LNA) circuit operating at frequencies of 900MHz and 1000MHz. then it will convert the components of the LNA circuit into a distributed strip circuit using specialized software (Microwave Office-MWO). Additionally, we will compare the results from the simulations with their potential practical counterparts.

2. LNA Design Stages

Designing a low noise amplifier requires some necessary preparatory stages and analytical processes starting from choosing the appropriate type of transistor and matching circuits in the input and output as well as the type of design and purpose of its work in addition to choosing the type of insulating material used (substrate), in addition to the type of connection used for the elements in the matching circuits and then analyzing the initial test results such as stability and working bias to reach the best results. The width of the transmission lines used in the amplifier circuit was calculated and some programs prepared for this purpose were used.

To ensure the signal is transmitted at the largest possible value from the input to the output, the reflection coefficients (S11, S22) must be as low as possible, as it may be possible to transfer a certain power from a load source at a certain frequency, but it is difficult to transfer and regulate it without loss, so the condition that must be met for the maximum power to be transferred from the source to the output is that the source impedance is equal to the compound conjugate of the load impedance. The design of LNA requires the use of complex techniques in designing matching circuits, including. The first technique in which the intensity of the signal entering the amplifier is controlled. This process requires a matching circuit that changes the input signal with the frequency, resulting in an almost constant output. The matching circuit is of the lossless type, i.e. it does not contain resistors and depends in its operation on the reflected loss resulting from the power entering the transistor, i.e. on high values of (VSWR), in other words, controlling the values of mismatch (Loss Mismatch) to obtain the required properties [6]. Another technique is to add a matching circuit with losses (i.e. on resistors) and it must be designed to give the lowest possible (VSWR) over the required frequency range in order to obtain a reflected power equal to zero and in order to have the specifications of reducing loss with frequency. A matching circuit is added that compensates for the internal loss that increases with the increase in frequency of the transistor over the width of the band. This circuit usually consists of an ohmic circuit (with at least one resistor). The purpose of this design is that the power gain at low frequencies of the beam is reduced by using ohmic losses, thus obtaining a lower VSWR and determining the required gain.

2.1 Two-Stage LNA Circuit with BJT at 900 MHz

A circuit was designed to operate with two stages of amplification using a BJT transistor (T605108). The stages of matching and conversion to a distributed circuit were completed, and the results were extracted. (see Fig 1).

2.2 Two-Stage LNA Circuit Using BJT at 1 GHz

The circuit was also configured with two stages, employing a different BJT transistor (BFG520XI). The stages of matching and conversion to a distributed circuit were performed, nd the results were gathered. (see Fig 2).

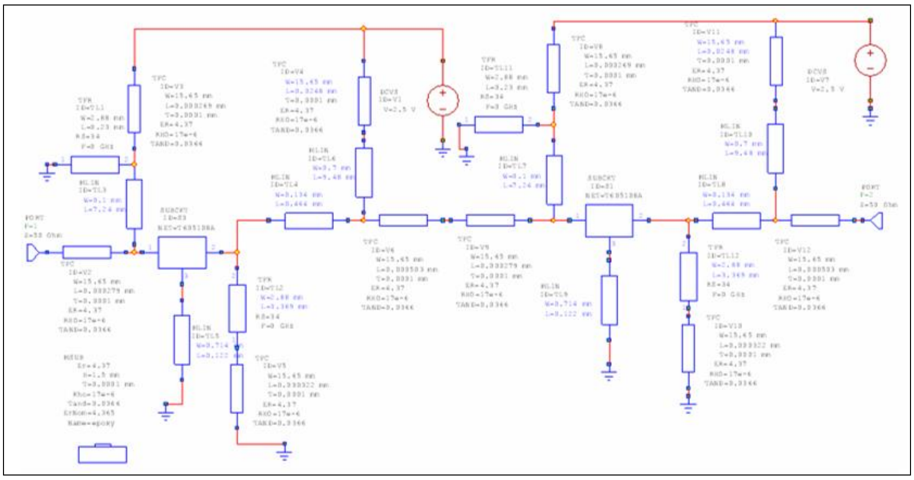


Fig 1: The two-stage LNA distributed circuit type JBT at 900MHz

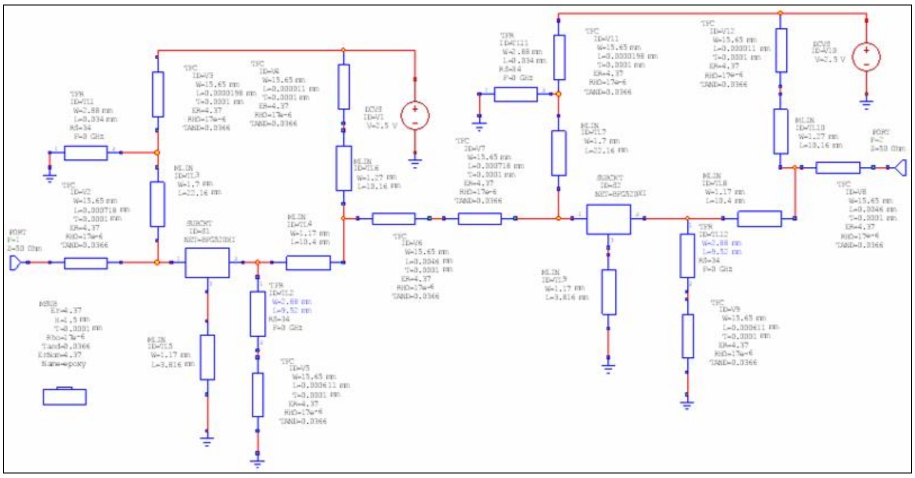
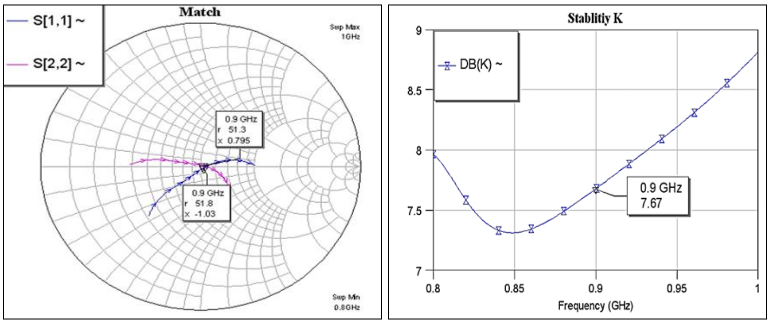


Fig 2: The two-stage LNA distributed circuit type JBT at 1000MHz



a b

Fig 3: The output results for the two-stage LNA type BJT at 900MHz (a. Matching on Smith's chart, b. Stability K)

3. Results and Discussion

The output results of the distributed LNA circuit at a frequency of 900MHz by choosing the BJT for two stages in Fig 1, were shown in Figures (3) and (4):

Figure (3-a) shows the value obtained for the matching when simulating the circuit for both the input and output impedance close to (50Ω) and it is clear that the circuit performance is good at this frequency, which means that the input circuit is compatible with the transistor input, on the other hand the transistor output is also compatible with the circuit output. As for the stability coefficient K for the two-stage distributed circuit that operates with a (BJT) transistor, its value was (7.6) at 900MHz, as shown in Figure (3-b).

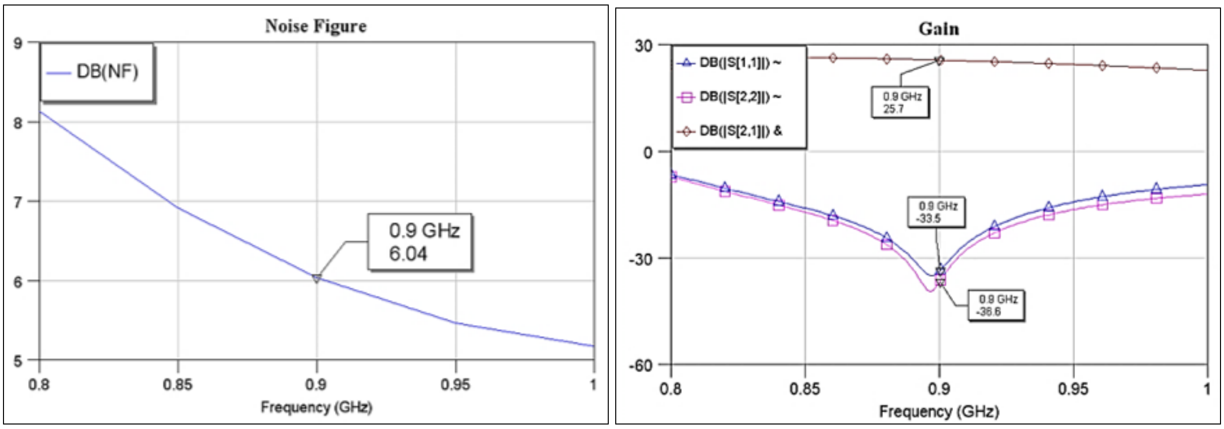


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Fig 4: The output results for the two-stage LNA type BJT at 900MHz (a. The Noise Figure, b. Reflection Coefficients)

Figure (4-a) shows that the input reflection coefficient S11 was (-33.5dB) at 900MHz, while the output reflection coefficients S22 was (-36.5dB) at 900MHz [7]. The forward gain coefficient S21 increased to (25.7dB) at 900MHz suggesting that the signal is being amplified effectively [8]. And noise figure value was (~6dB) at 900MHz, see Figure (4-b). A lower noise figure is crucial for preserving the signal-to-noise ratio. A noise figure of around 6dB is acceptable for some applications but could be improved for more sensitive receivers [9].

Now the output results of the distributed LNA circuit at 1000MHz by choosing the BJT for two stages in Fig 2, were shown in Figures (5) and (6):

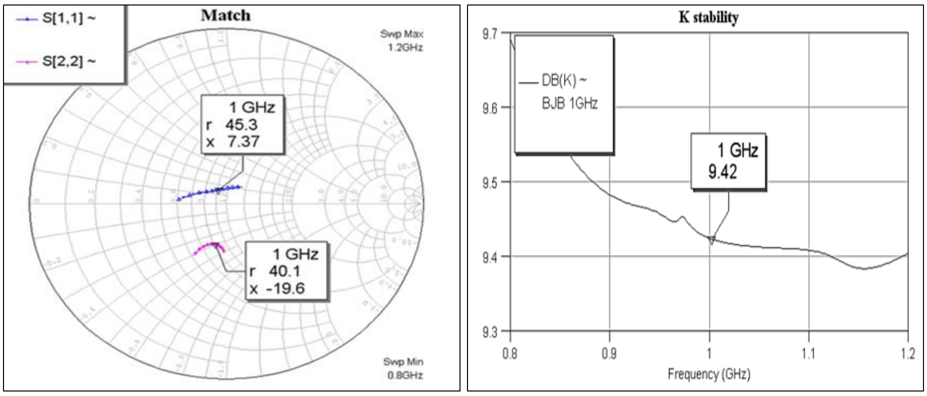

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Fig 5: The output results for the two-stage LNA type BJT at 1000MHz (a. Matching on Smith's chart, b. Stability K)

The performance of the two-stage distributed BJT circuit at 1000MHz was evaluated as shown in Figure 5, Figure (5-a) shows the value obtained for the matching when simulating the circuit for both the input and output impedance close to (50Ω), and it is clear that the circuit performance is good at this frequency. Furthermore, the stability factor (K) for the circuit at 1GHz was calculated to be 9.42, as illustrated in Figure (5-b). The stability factor (K) is significantly greater than 1. This high K value indicates that the amplifier is unconditionally stable at this frequency. This is a crucial design requirement, ensuring that the amplifier will not oscillate under any passive load conditions. This high stability margin suggests a robust design from a stability perspective.

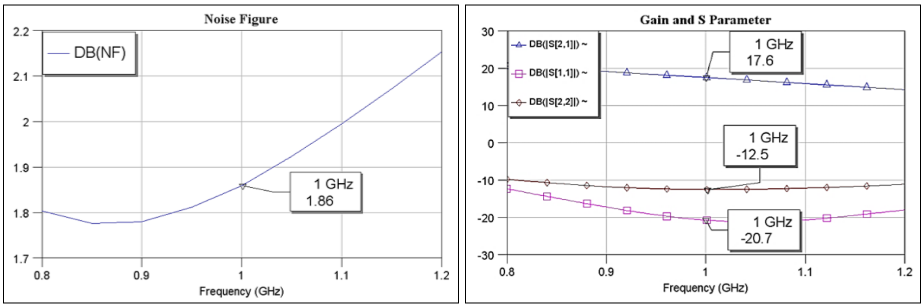

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Fig 6: The output results for the two-stage LNA type BJT at 1000MHz (a. The Noise Figure, b. Reflection Coefficients)

From Figure (6-a) the input reflection coefficient S11 was measured at (-20.7dB), and the output reflection coefficient S22 was (-12.5dB). The forward gain S21 at 1000MHz was observed to be (17.6dB). The presented results offer insights into the performance characteristics of the two-stage distributed BJT circuit at the operating frequency of 1000MHz. This higher value indicates a greater proportion of power being reflected from the output, potentially impacting power transfer efficiency to the load.

The comparison was made between the combined and distributed circuit at frequencies 900MHz and 1*000*MHz, which were obtained and the results were listed in Tables 1.

Table 1: Comparison of the main output simulation results of a two-stage amplifier when using the insulation layer thickness h = 1.5mm and εr = 4.37

LNA	Work type	Transistor	Frequency (MHz)	Gain (dB)	Noise Figure (dB)	Stability (dB)
Two stage	**Simulation**	**BJT**	**900**	**25.7**	**4.6**	**7.6**
Two stage	**Simulation**	**BJT**	**1000**	**17.6**	**1.8**	**9.4**

The table presents a comparison of key performance metrics for a two-stage BJT low-noise amplifier (LNA) at 900 MHz and 1000 MHz, simulated with a fixed substrate thickness (h = 1.5mm) and relative permittivity (εr = 4.37). Several observations can be shown:

The gain of the LNA decreases as the frequency increases. At 900 MHz, the gain is 25.7 dB, while at 1000 MHz, it drops to 17.6 dB. As explained by Pozar [7], the gain roll-off at higher frequencies can be attributed to the frequency dependence of transistor parameters, as well as parasitic capacitances and inductances within the transistor and the surrounding circuitry. These parasitic elements become more significant at higher frequencies, limiting the amplifier's ability to amplify the signal effectively. The noise figure shows a significant decrease with increasing frequency, this is an unusual observation, as typically, the noise figure either increases or remains relatively constant with increasing frequency, as discussed in Razavi explainsion [12]. It's possible that the matching network designed for 1000 MHz also provides better noise matching (i.e., presents an impedance to the transistor that minimizes noise contribution) compared to the matching network at 900 MHz. Another possibility is that the dominant noise mechanisms within the BJT change with frequency, as explained by Vendelin *et al.* [9]. The stability factor (K) increases with frequency, as (K) value greater than 1, for both frequencies, indicates unconditional stability, meaning the amplifier will not oscillate under any passive load conditions, as detailed in Pozar [7]. The increase in K with frequency suggests that the amplifier becomes even more stable at the higher frequency.

4. Conclusion

- Focus on minimizing parasitic elements and optimizing the matching network to maintain higher gain at higher frequencies.
- Ensure careful optimization of the matching network and explore methods to minimize noise across a wider frequency range.
- Continue designing to maintain a stability factor above 1, ensuring reliable operation across all conditions.

5. Acknowledgements

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